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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO		
09/941,484	08/28/2001	Ali Muhtaroglu	Ali Muhtaroglu 42390.P10961			
75	590 01/02/2004	EXAMINER				
Jan Carol Littl	<del></del>	TABONE JR, JOHN J  ART UNIT PAPER NUMBER 2133				
BLAKELY, SC Seventh Floor	OKOLOFF, TAYLOR & 2					
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Los Angeles, C	CA 90025-1026		DATE MAILED: 01/02/2004			

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary			Application No.		Applicant(s)			
			09/941,484	MUHTAROGLU, ALI				
		ļ	Examiner		Art Unit			
			John J Tabone, Jr.		2133			
Period fo	The MAILING DATE of this communication Reply	ition appe	ears on the cover sheet w	vith the co	orrespondence address			
THE - Exte after - If the - If NO - Failu - Any	ORTENED STATUTORY PERIOD FOR MAILING DATE OF THIS COMMUNIC/ nsions of time may be available under the provisions of SIX (6) MONTHS from the mailing date of this communical period for reply specified above is less than thirty (30) of period for reply is specified above, the maximum statuth reto reply within the set or extended period for reply will reply received by the Office later than three months after the patent term adjustment. See 37 CFR 1.704(b).	ATION.  37 CFR 1.136 ication. days, a reply ory period will, by statute, o	6(a). In no event, however, may a within the statutory minimum of thi paphy and will expire SIX (6) MO cause the application to become A	reply be time irty (30) days NTHS from t ABANDONED	ely filed will be considered timely. he mailing date of this communication. 0 (35 U.S.C. § 133).			
1)⊠	Responsive to communication(s) filed	on <u>28 Au</u>	gust 2001.					
2a) <u></u>	☐ This action is <b>FINAL</b> . 2b)☑ This action is non-final.							
3)□	3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under <i>Ex parte Quayle</i> , 1935 C.D. 11, 453 O.G. 213.							
Disposit	ion of Claims							
5)□ 6)⊠ 7)⊠	<ul> <li>Claim(s) 1-32 is/are pending in the application.</li> <li>4a) Of the above claim(s) is/are withdrawn from consideration.</li> <li>Claim(s) is/are allowed.</li> <li>Claim(s) 1-13,17-20, 26, 30 is/are rejected.</li> <li>Claim(s) 14-16,21-25,27-29,31 and 32 is/are objected to.</li> <li>Claim(s) are subject to restriction and/or election requirement.</li> </ul>							
	ion Papers	,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,	orodion roquiromoni.					
	The specification is objected to by the E	Evaminer						
	The drawing(s) filed on <u>28 August 2003</u>			biected to	o by the Examiner.			
-,_	Applicant may not request that any objection	-		•	•			
	Replacement drawing sheet(s) including th	e correction	on is required if the drawing	g(s) is obje	ected to. See 37 CFR 1.121(d).			
11)[	The oath or declaration is objected to b	y the Exa	aminer. Note the attache	ed Office	Action or form PTO-152.			
Priority (	under 35 U.S.C. §§ 119 and 120							
* 5 13)	Acknowledgment is made of a claim for All b) Some * c) None of:  1. Certified copies of the priority do a. Copies of the certified copies of application from the International Acknowledgment is made of a claim for ince a specific reference was included in 7 CFR 1.78.  Acknowledgment is made of a claim for ince a claim for ince a specific reference was included in the foreign language.	ocuments the priori al Bureau for a list of domestic n the first uage providomestic	have been received. have been received in a ty documents have been (PCT Rule 17.2(a)). If the certified copies no priority under 35 U.S.C. Is sentence of the specific visional application has to	Application received to received to the second to the seco	on No d in this National Stage  d. ) (to a provisional application) in an Application Data Sheet. eived. and/or 121 since a specific			
Attachmer			_					
2) D Notic	ce of References Cited (PTO-892) ce of Draftsperson's Patent Drawing Review (PTC mation Disclosure Statement(s) (PTO-1449) Pap	•	5) 🔲 Notice of		(PTO-413) Paper No(s) atent Application (PTO-152)			

Application/Control Number: 09/941,484 Page 2

Art Unit: 2133

#### **DETAILED ACTION**

1. Claims 1-32 have been examined.

# **Drawings**

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: In Figure 1, the Reference Voltage Regulator 106 as sited on page 7, line 7 is missing the label 106. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

# Specification

- 3. The specification is objected to as failing to include a <u>Brief Summary of the Invention</u>: See MPEP § 608.01(d). A brief summary or general statement of the invention as set forth in 37 CFR 1.73. The summary is separate and distinct from the abstract and is directed toward the invention rather than the disclosure as a whole. The applicant is requested to include a <u>Brief Summary of the Invention</u> on page 3 at line 16.
- 4. The specification is objected to because of the following informalities: missing period, page 3, line 14. The configuration bits 152 should be numbered 150, page 9, line 1. Appropriate correction is required.

Claim Rejections - 35 USC § 112

Art Unit: 2133

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claim 5, 6, 7, 26-29 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

# Claim 5:

The phrase further comprising second logic <u>coupled</u> to open and close the set of switches... is indefinite and of wrong use. It is not clear by this claim what the second logic is coupled to. Correction is requested.

#### Claim 26:

It is not clear where the configuration bits come from: the first number of input pins or second number.

The relationship between the first input pins and second input pins is unclear. Further disclosure is requested.

### Claims 6, 7, 27-29:

These claims are rejected because they depend on 5 and 26 and contain the same problems of indefiniteness.

6. Claim 5, 6, 12 and 13 rejected under 35 U.S.C. 112, second paragraph, for insufficient antecedent basis.

<u>Claim 5</u> recites the limitation "the set of switches" in claim 1. There is insufficient antecedent basis for this limitation in the claim. The set of switches are disclosed in

claim 3 not in claim 1. For the purpose of further examination, the examiner will interpret claim 5 as reading "The integrated circuit of claim 3". Correction is required.

Claims 12 and 13 recite the limitation "set of analog voltages" in claim 8. There is insufficient antecedent basis for this limitation in the claim. For the purpose of further examination, the examiner will interpret claim 12 and 13 as reading "set of DC voltages" in the place of "set of analog voltages". Correction is required.

# Claim 6:

This claim is rejected because it depends on claim 5 and contains the same problems of insufficient antecedent basis.

# Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

- (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- 7. Claims 1-4, 8-11, 17-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matthews (US-5600247).

#### Claims 1 and 17:

Matthews teaches of a Digital-to-Analog Converter (DAC) 80 for creating a DC voltage. Matthews teaches of a comparator 84 for comparing the DC voltage and a reference voltage. (See col.6, lines 33-42). Matthews does not explicitly teach the interpretation of the comparator 84 outputs, however, Matthews discloses the comparator 84 outputs

Art Unit: 2133

(EDV outputs) are coupled to the microcontroller 64 and are used in internal decision making to present information to the display. (See Figure 4, col. 9, lines 10-21, col. 18, lines 4-9). It would have been obvious to one of ordinary skill in the art at the time the invention was made that Matthews' internal decision making would encompass an interpreting process for interpreting the outputs (EDV states) from the comparator (84). On having ordinary skill in the art would be motivated to do so because Matthews teaches the outputs (EDV states) of the comparator (84) may be presented on the display (col. 9, lines 13-16).

# Claim 8:

Matthews teaches of a Digital-to-Analog Converter (DAC) 80 for creating a DC voltage. Matthews teaches of a comparator 84 for comparing the DC voltage and a reference voltage. (See col.6, lines 33-42). Matthews does not explicitly teach the interpretation of the comparator 84 outputs, however, Matthews discloses the comparator 84 outputs (EDV outputs) are coupled to the microcontroller 64 and are used in internal decision making to present information to the display. (See Figure 4, col. 9, lines 10-21, col. 18, lines 4-9). It would have been obvious to one of ordinary skill in the art at the time the invention was made that Matthews' internal decision making would encompass an interpreting process for interpreting the outputs (EDV states) from the comparator (84). On having ordinary skill in the art would be motivated to do so because Matthews teaches the outputs (EDV states) of the comparator (84) may be presented on the display (col. 9, lines 13-16). Matthews further teaches that the negative input of the comparator 84 is connected to the output of a multiplexer 86.

Art Unit: 2133

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Further, a TEMP signal is input to the multiplexer 86, which TEMP signal represents a temperature variable voltage that is generated in the band gap reference circuit 78 and provides an indication of temperature. (See Figure 4, col.6, lines 39-49).

# Claims 2, 9, 18:

Matthews teaches the DAC 80 has digital input connected to the bus 66 to receive a data word, which represents a voltage level that is generated by the microcontroller 64. This converted to an analog voltage by the DAC 80. (See col. 6, lines 33-37). It would have been obvious to one of ordinary skill in the art at the time the invention was made that the DAC 80 is responsive to the data word (configuration bits) to generate DC voltages.

#### Claims 3, 10, 19:

Matthews teaches the DAC 80 has digital input connected to the bus 66 to receive a data word, which represents a voltage level that is generated by the microcontroller 64. This converted to an analog voltage by the DAC 80 for input to the positive input of a comparator 84. (See col. 6, lines 33-39). It would have been obvious to one of ordinary skill in the art at the time the invention was made that the microcontroller 64 enables the analog voltage (DC voltage) to be applied to the non-inverting input of the comparator 84 (sense amplifier) by being coupled to the DAC 80 (voltage generator).

#### Claims 4, 11, 20:

Matthews teaches the DAC 80 has digital input connected to the bus 66 to receive a data word, which represents a voltage level that is generated by the

Art Unit: 2133

microcontroller 64. This is converted to an analog voltage on an output line 82 for input to the positive input of a comparator 84. (See col. 6, lines 33-39).

8. Claims 26 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Otsuji (US-4928278).

# Claim 26, 30:

Otsuji teaches of an IC test system that provides n pin electronics units corresponding to n input/output pins on an IC device (first number of input pins). Each pin electronics unit that includes a test pattern generator A, a waveform formatter circuit 3, a pattern generator 7 and a driver 4. A reference timing signal generator 11 is also provided which output is simultaneously supplied through a switch 16 arranged in each pin electronics unit to a group of signal lines by a signal distributor 14, each extending from each pin electronics unit 9-i to its corresponding input/output pin 1-i (i=1, 2, 3, ..., n) (a second smaller number of input pins) of the IC device 1 under test through switches 17 and 18 arranged in each pin electronics unit. (See col. 7, lines 40-68). Otsuji does not explicitly disclose a "levels generating circuitry", however, Otsuji does disclose a driver 4 that supplies the test signal pattern to the comparator 5 through the switch 17 and 16. (See col.8, lines 28-30). It would have been obvious to one of ordinary skill in the art at the time the invention was made that the driver 4 would have been named as the "levels" generating circuitry", which is also coupled to the pins via switches 17 and 18. The artisan would be motivated to do so because Otsuji's driver 4 also supplies levels to the comparator 5.

Art Unit: 2133

# Claim Objections

9. Claims 5-7, 12, 13 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action and to <u>include all</u> of the <u>limitations</u> of the base claim and any intervening claims.

10. Claims 14-16, 21-25, 27-29 and 31-32 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form <u>including</u> all of the <u>limitations</u> of the base claim and any intervening claims.

#### Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John J Tabone, Jr. whose telephone number is (703)305-8915. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (703)305-9595. The fax phone number for the organization where this application or proceeding is assigned is (703)305-3718.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)305-3900.

JJT (f)

CHRISTINE T. TU Primary Examiner Page 8